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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,450	06/01/2001	Michael I. Catherwood	18153.0034	8450

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,450	CATHERWOOD, MICHAEL I.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-24 are presented for examination.

2. The Information Disclosure Statement filed November 16, 2001 fails to comply with the provisions of MPEP § 609 because copies of the cited references have not been provided. In fact, the cover letter for the information disclosure statement admits that copies of the cited references have not been provided and are instead found in a list of other application numbers. Applicant is reminded of the provisions of 37 CFR 1.98(d) which states:

> "(d) A copy of any patent, publication, pending U.S. application or other information, as specified in paragraph (a) of this section, listed in an information disclosure statement is required to be provided, even if the patent, publication, pending U.S. application or other information was previously submitted to, or cited by, the Office in an earlier application, unless:
>
> (1) The earlier application is properly identified in the information disclosure statement and is relied on for an earlier effective filing date under 35 U.S.C. 120; and
>
> (2) The information disclosure statement submitted in the earlier application complies with paragraphs (a) through (c) of this section.

In order not to supply references along with an information disclosure statement, this application must have relied upon all of the listed other applications for an earlier effective filing date under 35 U.S.C. 120, which this application does not rely on any prior application for any effective filing date. Therefore, because this application does not claim priority under 35 U.S.C. 120, copies of the references were required to be submitted.

The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements. See MPEP § 609 (c)(1).

3. Applicant is advised that should claim 4 be found allowable, claim 5 will be objected to under 37 CFR1.75 as being a substantial duplicate thereof. When who claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

4. The following in a quotation of the first paragraph of 35 USC 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-24 are rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed invention is directed to executing a "find first bit" instruction which locates a first bit within a data word having a particular state. However, the level of disclosure provided by the specification does not indicate that applicant had possession of the claimed invention. The disclosure of how to actually accomplish this "find first bit" instruction amounts to mere statements that the instruction is executed, and that the bit is found, without providing any details as to how to go about actually implementing the "find" part of "find first bit". For example, see fig. 4 where box 440 simply states "execute the bit operation" without giving any details of how that "execution" is accomplished. Figure 6 contains a blank box 600 containing only the label "find first logic". There is no disclosure of the logic within box 600 which performs the "find first" function, and as the "find first" function of box 600 is critical to performing the claimed instruction operation, it's omission amounts to an indication that the inventors, at time of invention, did not themselves have possession of the requisite logic within box 600 that performs the "find first" function. The written specification is similarly lacking in description of the structure and function of the "find first logic" of box 600. The specification spends seven pages (pg. 6-13) describing basic processor background architecture and yet devotes only 18 lines on page 13 to describing the "find first" aspects of the invention, the description amounting to little more than "the ALU performs the operation". Furthermore, about half of those 18 lines again describe conventional processor architecture techniques amounting to little more than "instructions contain source and destination operand specifier values". On pg. 14, figure 4 is described, and the totality of the description given for box 440 is exactly: "In step 440, the processor executes the bit operation instruction decoded." This simply states that the function is performed (which is merely an inherent statement, because unless it is performed, no operation happens) but provides no details as to **how** to perform this function. This is further evidence that the

inventors did not have possession of the knowledge of **how** to perform this function, because had they had possession of this knowledge, they are required by law to disclose it upon filing a patent application. The description of figure 6 begins on line 16 of page 14 and ends at line 13 of page 15. Again the description of box 600, which knowledge of the internal functionality is critical to the invention, is simply:

> "When a find first instruction is decoded, the instruction decoder 620 sends control signals to the find first logic to cause the find first logic to perform a masking operation on the value received from the register 330 which in the illustrative embodiment is a 16 bit value. The masking operation performed is determined by the particular type of find first instruction. In general, the masking operation may produce a value of all zeros except for the bit position occupied by the first zero (or one) from the left or right or the first bit change depending on the instruction"

This description states the input to the find first logic receives a 16 bit value, that it performs a mysterious "masking operation", and that it outputs a value having all zero bits except for the particular bit that the instruction was operating upon. However, this description fails to describe how the "masking operation" performs this mysterious feat of consuming a 16 bit quantity and mysteriously outputting a value of all zeros except for the desired bit. Lack of description of this mysterious "masking operation" is further evidence that the inventors did not have possession of this critical element of the invention at the time of filing for a patent.

6. Claims 1-24 are rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As described, supra. in regards to the inventors not having possession of a critical element of the invention at time of filing, this lack of disclosure of **how** to actually perform the "find first" operation also presents a non-enabling disclosure of the invention. Because the description of the "find first" logic amounts to "the logic finds the first bit", one of ordinary skill in the art would be unable to make and/or use the invention because the critical key component necessary to perform the invention has not been disclosed. Without disclosure of the internal operation and function of "find first logic" (600), it is impossible to make and/or use the invention claimed in this application without undue experimentation on the part of one of skill in the art. Therefore, the omission of this critical element of the invention from the application results in a lack of enablement of the claimed invention.

7. Claim 8 is rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7.1. The following terms lack proper antecedent basis:

7.1.1. "the find first one instruction" claim 8;

8. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

10. Claims 1-3, 6, 9, 11-16, 18-19, 21-22, and 24 are rejected under 35 USC § 102(b) as being clearly anticipated by *Digital VAX 11/780 Architecture Handbook* ("Digital"), copyright 1977, Digital Equipment Corporation.

Digital taught (e.g. see pgs. 7-16 to 7-17) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

10.1. a method of processing a bit operation instruction (pg. 7-16, "FIND FIRST"), comprising;

10.2. fetching and decoding (it is inherent that the VAX CPU will both fetch and decode instructions) a find first bit instruction ("FIND FIRST");

10.3. executing (it is inherent that the VAX CPU will execute the instruction) the find first bit instruction on a source operand (base.ab) to calculate a result (findpos.wl) corresponding to the first bit position meeting the criteria of the instruction (pg. 7-16, Description section);

10.4. storing the result (pg. 7-16, Description, "If a bit in the indicated state is found, the

find position operand is replaced by the position (relative to the base) of a bit one position to the left of the specified field").

11. As to claim 2, Digital taught further comprising setting a zero flag within a status register when none of the bit positions meet the criteria of the instruction (pg. 7-17, Condition Codes, "Z <- {bit not found};").

12. As to claim 3, Digital taught that the instruction was a find first zero instruction (Opcodes, "Find First Clear").

13. As to claim 6, Digital taught that the instruction was a find first one instruction (Opcodes: "Find First Set").

14. As to claim 9, Digital taught that the instruction was a find first bit change instruction ("Find First Clear", "Find First Set").

15. As to claim 11, Digital taught that the find first bit change instruction finds the first bit change from the right side of a memory location (see figure under "Operation").

16. As to claim 12, Digital taught that the find first bit instruction specifies the source operand ("base.ab").

17. As to claim 13, Digital taught that the find first bit instruction specifies (base.ab) a byte of a memory location that stores the source operand (pg. 3-2, "The basic addressable unit in VAX11 is the 8-bit byte").

18. As to claims 14-16, 18-19, 21-22, and 24, they do not teach or define above the invention claimed in claims 1-3, 6, 9, 11, and 12-13 and are therefore rejected under Digital for the same reasons set fourth in the rejection of claims 1-3, 6, 9, 11, and 12-13, supra.

19. Claims 4-5, 7-8, 10, 17, 20, and 23 are rejected under 35 USC § 103 as being unpatentable over Digital, as applied to claims 1-3, 6, 9, 11, and 12-13, supra., in view of *Intel Pentium Processor Family Developer's Manual, Volume 3, Architecture and Programming Manual*, 1995, Intel Corporation.

20. As to claims 4-5, 7-8, 10, 17, 20, and 23 Digital did not teach that the instruction operated from the left side of a memory location. However, Intel taught a pair of instruction (pg. 4-12, BSF, BSR) which together implemented scanning for set bits from both the left side and right sides of memory locations (Bit Scan Forward - scans low-to-high (from bit 0 toward

the upper bit positions), Bit Scan Reverse - scans high-to-low (from the uppermost bit toward bit 0). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized Intel's teachings of scanning for bits from both the left and right sides of a memory word to modify Digital to additionally scan from the left side of a memory location in addition to it's native scanning from the right side of a memory location. One of ordinary skill in the art would have been motivated to provide both from the left and from the right side scanning because doing so provides greater flexibility to the programmer by allowing him/her to setup their data structures in the arrangement they desire, while still allowing easy use of those data structures by simply selecting the correct direction of scanning for location of set/clear bits.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US2002/0,194,233 discloses a system for performing bit searches within a data word.

5,568,410 discloses a system for finding the number of leading zero bits or one bits of a data word.

5,349,681 discloses a system for searching for bits within a data word.

3,430,208 discloses a system for determining the bit position of a least significant bit having a predetermined value.

22. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

Richard Ellis
May 25, 2004